

## High CMTI, 3A Source and 6A Sink Reinforced Isolated Single Channel Gate Driver with Split Output and Active Protection Features

### GENERAL DESCRIPTION

The SiLM5852SH-AQ is an advanced single channel isolated gate driver with split output and active protection features, such as desaturation detection, UVLO, isolated fault sensing and active miller clamp. Its peak output current is 3A for source and 6A for sink.

The input side supply operates from 3V to 5.5V and the output side supply allows for a range from 13V to 30V. All the supply voltage pins have under voltage lock-out (UVLO) protection.

An internal desaturation (DESAT) fault detection recognizes when the IGBT is in an overcurrent condition. When desaturation is active, a fault signal is sent across the isolation barrier, pulling the **FAULT** output low at the input side and blocking the isolator input. When the IGBT is turned off during normal operation with bipolar output supply, the output is clamped to VEE2. If the output supply is unipolar, an active Miller clamp can be used, allowing Miller current to sink across a low impedance path, preventing IGBT to be dynamically turned on during high voltage transient conditions. The input side is isolated from output driver by a 5kV<sub>RMS</sub> reinforced isolation barrier, with a minimum of 150kV/us common-mode transient immunity (CMTI).

### APPLICATION

- AC and brushless DC motor drives
- Renewable energy inverters
- Industrial power supplies

### FEATURES

- AEC-Q100 qualified for automotive application
  - Temperature grade 1: -40°C to +125°C, T<sub>A</sub>
- 3A source and 6A sink output current with split output
- 2.5A active Miller clamping
- 185mA soft turn-off during short circuit
- Desaturation detection
- Fault alarm upon desaturation and reset from **RST**
- Input and Output UVLO with RDY pin indication
- Active output pulldown and default low output with low supply or floating inputs
- CMOS compatible inputs
- Reject input pulses and noise transients shorter than 30ns
- 90ns (Typ) propagation delay
- 150kV/us (Min) common mode transient immunity (CMTI)
- Input side supply range from 3V to 5.5V
- Output side supply range from 13 V to 30 V
- SOP16W package with >8.0mm creepage and clearance
- Operating junction temperature: -40°C to +150°C
- Safety certifications
  - 5kV<sub>RMS</sub> isolation for 1 minute per UL 1577
  - CQC certification per GB4943.1-2022
  - DIN VDE 0884-17: 2021-10 (Pending)

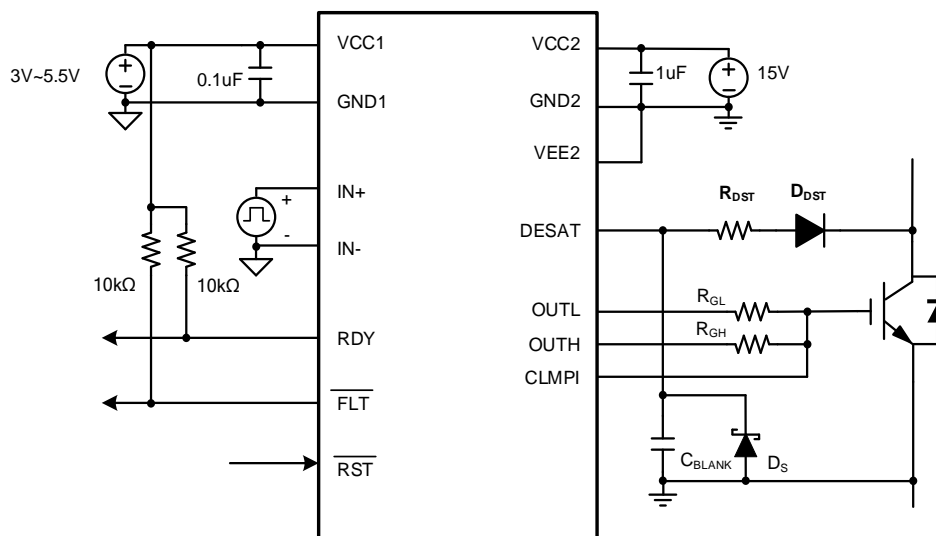


Figure 1. SiLM5852SH-AQ Application Circuit to Driver IGBT

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## PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP16W	<p>Pin 1: VEE2 Pin 2: DESAT Pin 3: GND2 Pin 4: OUTH Pin 5: VCC2 Pin 6: OUTL Pin 7: CLMPI Pin 8: VEE2 Pin 9: GND1 Pin 10: IN+ Pin 11: IN- Pin 12: RDY Pin 13: <math>\overline{\text{FLT}}</math> Pin 14: <math>\overline{\text{RST}}</math> Pin 15: VCC1 Pin 16: GND1</p>

## PIN DESCRIPTION

No.	Pin	Description
1	VEE2	Negative supply rail for driver voltage
2	DESAT	Desaturation current protection input. If not used, short to GND2
3	GND2	Common ground reference, connecting to emitter pin of IGBT or source pin of SiC/MOSFET
4	OUTH	Driver output pull up
5	VCC2	Positive supply rail for driver voltage
6	OUTL	Driver output pull down
7	CLMPI	Internal active miller clamp. If not used, short to VEE2
8	VEE2	Negative supply rail for driver voltage
9	GND1	Input power supply and logic ground reference
10	IN+	Non-inverting driver control input
11	IN-	Inverting driver control input. If not used, short to GND1
12	RDY	Power good for input and output side power supply. It is open drain configuration and can be paralleled with other RDY signals
13	$\overline{\text{FLT}}$	Active low fault output upon over current detection. It is open drain configuration and can be paralleled with other fault signals
14	$\overline{\text{RST}}$	Reset input, apply low pulse to reset fault latch
15	VCC1	Input power supply
16	GND1	Input power supply and logic ground reference

FUNCTIONAL BLOCK DIAGRAM

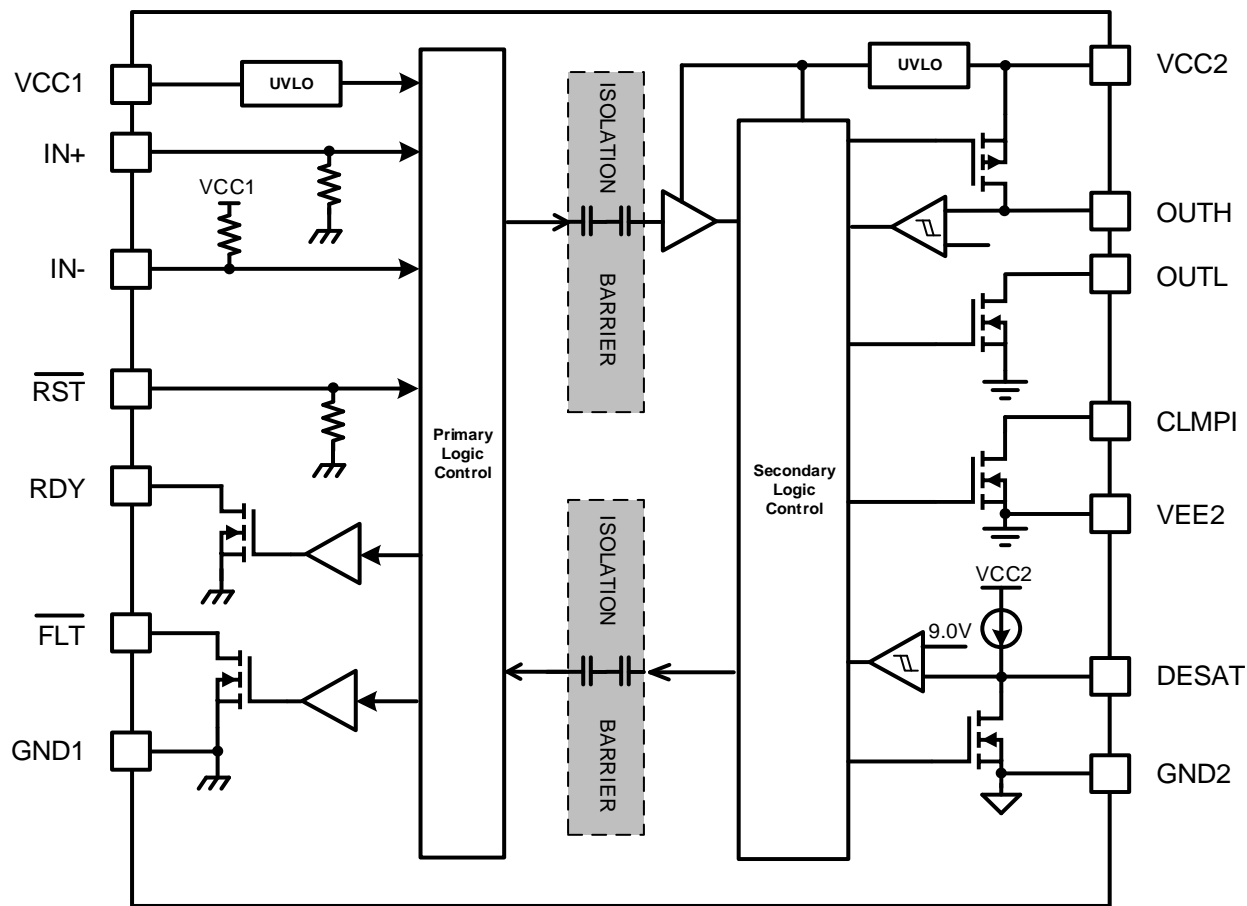


Figure 2. SiLM5852SH-AQ Block Diagram

**ORDERING INFORMATION**

Order Part No.	Package	QTY
SiLM5852SHCG-AQ	SOP16W, Pb-Free	1500/Reel

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Definition	Min	Max	Units
VCC1 -GND1	Input Side Supply Voltage	-0.3	6	V
VCC2 -VEE2	Output Side Supply Voltage	-0.3	33	V
VEE2 -GND2	Negative Output Supply Voltage	-20	0.3	V
VCC2 -GND2	Positive Output Supply Voltage	-0.3	33	V
DESAT	Refer to GND2	GND2-0.3	Min(GND2 + 20, VCC2+0.3)	V
OUTH, OUTL, CLMPI		VEE2-0.3	VCC2+0.3	V
RDY, $\overline{\text{FLT}}$		GND1-0.3	VCC1	V
IN+, IN-, $\overline{\text{RST}}$		GND1-2	VCC1	V
$\overline{\text{IFLT}}$ , IRDY	Output current of $\overline{\text{FLT}}$ , RDY		20	mA
T <sub>J</sub>	Junction Temperature	-55	150	°C
T <sub>S</sub>	Storage Temperature	-65	150	

**RECOMMENDED OPERATION CONDITIONS**

Symbol	Definition	Min	Max	Units
VCC1 -GND1	Input Side Supply Voltage	3	5.5	V
VCC2 -VEE2	Output Side Supply Voltage	13	30	V
VEE2 -GND2	Negative Output Supply Voltage	-15	0	V
VCC2 -GND2	Positive Output Supply Voltage	13	30	V
T <sub>J</sub>	Junction Temperature	-40	150	°C
T <sub>A</sub>	Ambient Temperature	-40	125	°C

**ESD RATINGS**

Symbol	Definition	Value	Units
V <sub>ESD</sub>	HBM	±8000	V
	CDM	±2000	

**THERMAL INFORMATION<sup>1</sup>**

Symbol	Definition	Value	Unit
R <sub>θJA</sub>	Junction to ambient thermal resistance	100	°C/W
R <sub>θJC(TOP)</sub>	Junction to case (top) thermal resistance	40	°C/W

Note1: Standard JESD51-3 low effective thermal conductivity test board.

## PACKAGE SPECIFICATIONS

Symbol	Definition	Min	Typ	Max	Units
$R_{IO}$	Resistance (Input Side to Output Side)		$10^{12}$		$\Omega$
$C_{IO}$	Capacitance (Input Side to Output Side)		0.8		pF

## INSULATION SPECIFICATIONS

Symbol	Definition	Test Condition	Value	Units
CLR	External clearance	Shortest terminal to terminal distance through air	8.0	mm
CPG	External creepage	Shortest terminal to terminal distance across the package surface	8.0	mm
DTI	Distance through the insulation	Minimum internal gap	>18	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11), IEC 60112	>600	V
	Material Group		I	
	Overvoltage category	Rated mains voltages ≤600Vrms	I-III	
		Rated mains voltages ≤1000Vrms	I-II	
DIN V VDE 0884-11 <sup>(1)</sup>				
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage		1500	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum isolation working voltage	AC voltage (Sine wave)	1060	V <sub>RMS</sub>
		DC voltage	1500	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	60s	7000	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage	Test method per IEC62368, 1.2/50us waveform, V <sub>TEST</sub> =1.6 x V <sub>IOSM</sub>	6250	V <sub>PK</sub>
q <sub>pd</sub>	Apparent charge	Method b2: V <sub>pd(m)</sub> =1.875 x V <sub>IORM</sub> , tm=1 s	≤5	pC
	Climatic Category		40/125/21	
	Pollution Degree		2	
UL1577				
V <sub>ISO</sub>	Withstand Isolation Voltage	V <sub>TEST</sub> =V <sub>ISO</sub> , t=60s (qualification), V <sub>TEST</sub> =1.2 x V <sub>ISO</sub> , t=1s (100% production)	5000	V <sub>RMS</sub>

Note1: Certification pending

SAFETY RELATED CERTIFICATIONS

VDE	UL	CQC
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2022
Reinforced Insulation	Single protection, 5000 V <sub>RMS</sub>	Reinforced insulation, Altitude ≤ 5000m
Pending	File number: E521801	File number: CQC23001379622

SAFETY LIMITING VALUES

Symbol	Parameter	Condition	Value	Unit
I <sub>s</sub>	Safety input, output, or supply current	R <sub>θJA</sub> =100°C/W, V <sub>CC2</sub> -V <sub>EE</sub> = 15V, T <sub>J</sub> =150°C, T <sub>A</sub> =25°C	80	mA
		R <sub>θJA</sub> =100°C/W, V <sub>CC2</sub> -V <sub>EE</sub> = 30V, T <sub>J</sub> =150°C, T <sub>A</sub> =25°C	40	mA
P <sub>s</sub>	Safety input, output, or total power	R <sub>θJA</sub> =100°C/W, T <sub>J</sub> =150°C, T <sub>A</sub> =25°C	Input side	50
			Output side	1200
			Total	1250
T <sub>s</sub>	Maximum safety temperature		150	°C

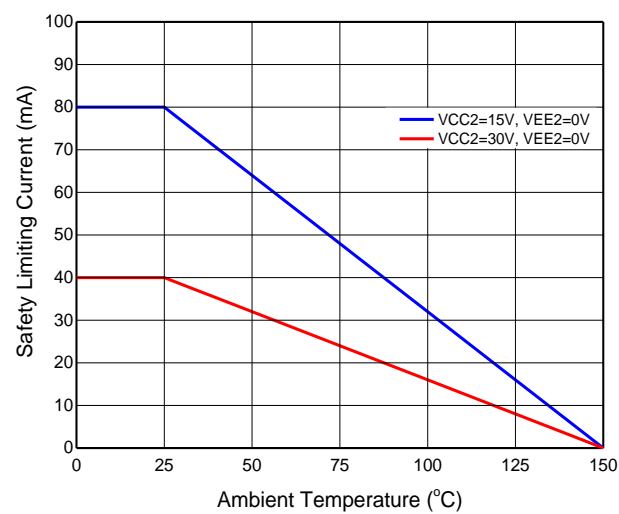


Figure 3. Thermal Derating Curve for Limiting Current per VDE

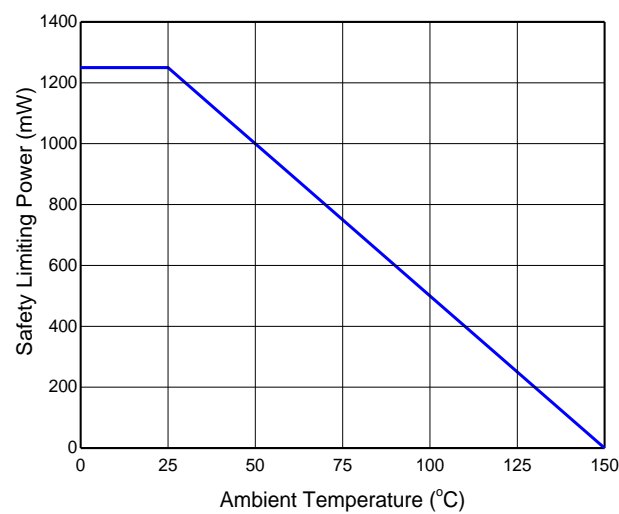


Figure 4. Thermal Derating Curve for Limiting Power per VDE



**ELECTRICAL CHARACTERISTICS (DC)**

All typical values at VCC1-GND1 = 5V, VCC2-GND2 = 15V, VEE2-GND2 = -8V and T<sub>A</sub> = 25°C unless otherwise specified. All min and max specifications are at recommended operating conditions and T<sub>A</sub> = -40°C to 125°C.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>UNDER VOLTAGE LOCKOUT</b>						
V <sub>UVLO1_R</sub>	Under Voltage Lockout Rising on VCC1			2.7	2.95	V
V <sub>UVLO1_F</sub>	Under Voltage Lockout Falling on VCC1		2.3	2.5		V
V <sub>UVLO1_HYS</sub>	Under Voltage Lockout Hysteresis on VCC1			0.2		V
V <sub>UVLO2_R</sub>	Under Voltage Lockout Rising on VCC2		10.5	11.7	13	V
V <sub>UVLO2_F</sub>	Under Voltage Lockout Falling on VCC2		9.5	10.8	12	V
V <sub>UVLO2_HYS</sub>	Under Voltage Lockout Hysteresis on VCC2			0.9		V
<b>Quiescent Current</b>						
I <sub>VCC1QL</sub>	VCC1 Quiescent Current	IN+ = GND1, IN- = VCC1		3.5	6	mA
I <sub>VCC2QL</sub>	VCC2 Quiescent Current	IN+ = GND1, IN- = VCC1		5.5	10	mA
I <sub>VCC1QH</sub>	VCC1 Quiescent Current	IN+ = VCC1, IN- = GND1		6	11	mA
I <sub>VCC2QH</sub>	VCC2 Quiescent Current	IN+ = VCC1, IN- = GND1		6.5	12	mA
<b>Logic IOs</b>						
V <sub>INH</sub>	Input High Threshold (IN+, IN-, $\overline{\text{RST}}$ )				70%	VCC1
V <sub>INL</sub>	Input Low Threshold (IN+, IN-, $\overline{\text{RST}}$ )		30%			VCC1
V <sub>IN_HYS</sub>	Input Hysteresis (IN+, IN-, $\overline{\text{RST}}$ )			15%		VCC1
I <sub>IH</sub>	High Level Input Leakage (IN+, $\overline{\text{RST}}$ )	IN+ = $\overline{\text{RST}}$ = VCC1	70	100	150	uA
I <sub>IL</sub>	Low Level Input Leakage (IN-)	IN- = GND1	-150	-100	-70	uA
V <sub>OL</sub>	Low Level Output Voltage ( $\overline{\text{FLT}}$ , RDY)	I = 5mA		100	200	mV
<b>Driver Stage</b>						
I <sub>OUTH</sub>	High Level Peak Output Current	IN+ = VCC1, IN- = GND1, VOUT = VCC2 - 15V	1.8	3		A

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I <sub>OUTL</sub>	Low Level Peak Output Current	IN+=GND1, IN-=VCC1, VOUT=VEE2+15V	3.6	6		A
V <sub>OH</sub>	High Level Output Voltage	IN+=VCC1, IN-=GND1, I <sub>O</sub> =-100mA		160	320	mV
V <sub>OL</sub>	Low Level Output Voltage	IN+=GND1, IN-=VCC1, I <sub>O</sub> =100mA		63	135	mV
V <sub>OUTPD</sub>	Active Output Pulldown Voltage	I <sub>OUT</sub> =200mA, VCC2 open			2.7	V
<b>Miller Clamp</b>						
V <sub>CLPTH</sub>	Clamp threshold voltage		1.8	2	2.2	V
V <sub>CLP</sub>	Clamp low level voltage	IN+=GND1, IN-=VCC1, I <sub>CLMPI</sub> =200mA		165	250	mV
I <sub>CLP</sub>	Clamp low sink current	IN+=GND1, IN-=VCC1, V <sub>CLMPI</sub> =VEE2+2.5 V	1.3	2.5		A
<b>Short Circuit Clamping</b>						
V <sub>CLP-OUTH</sub>	Clamping Voltage (OUTH – VCC2)	IN+=GND1, IN-=VCC1, I <sub>OUTH</sub> = 500mA, t <sub>CLP</sub> =10us		0.9	1.1	V
V <sub>CLP-OUTL</sub>	Clamping Voltage (OUTL – VCC2)	IN+=VCC1, IN-=GND1, I <sub>OUTL</sub> = 500mA, t <sub>CLP</sub> =10us		1.1	1.4	V
V <sub>CLP-CLMPI</sub>	Clamping Voltage (CLMPI – VCC2)	IN+=VCC1, IN-=GND1, I <sub>CLMPI</sub> = 500mA, t <sub>CLP</sub> =10us		1.2	1.5	V
<b>DESAT Protection</b>						
I <sub>CHG</sub>	blanking capacitor charge current	DESAT-GND2=2V	0.38	0.48	0.58	mA
I <sub>DCHG_DESAT</sub>	blanking capacitor discharge current	DESAT-GND2=6V	9	14	19	mA
V <sub>DSTH</sub>	DESAT threshold voltage with respect to GND2		8	9	10	V
V <sub>DSL</sub>	DESAT voltage with respect to GND2 when OUT is low	I <sub>DESAT</sub> =1mA			0.8	V
<b>Soft Turn-Off</b>						
I <sub>OLF</sub>	Low Level output current during fault condition (soft turn off)		100	185	270	mA

**SWITCHING CHARACTERISTICS (AC)**

All typical values at VCC1-GND1 = 5V, VCC2-GND2 = 15V, VEE2-GND2 = -8V and T<sub>A</sub> = 25°C unless otherwise specified. All min and max specifications are at recommended operating conditions and T<sub>A</sub> = -40°C to 125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t <sub>PLH</sub>	Propagation delay, Low to High	C <sub>LOAD</sub> =1nF, f <sub>sw</sub> =20kHz, (50% Duty Cycle), V <sub>CC2</sub> =15V		90	130	ns
t <sub>PHL</sub>	Propagation delay, High to Low			90	130	ns
t <sub>PWD</sub>	Pulse Width Distortion				35	ns
t <sub>sk-pp</sub>	Part to Park skew				35	ns
t <sub>r</sub>	Turn on rise time	C <sub>LOAD</sub> =10nF		54		ns
t <sub>f</sub>	Turn off fall time			30		ns
t <sub>UVLO1_REC</sub>	VCC1 UVLO Recovery Delay	VCC1 Rising from 0V to 5V		15	25	us
t <sub>UVLO2_REC</sub>	VCC2 UVLO Recovery Delay	VCC2 Rising from 0V to 15V		40	60	us
t <sub>VCC1+_RDY</sub>	VCC1 UVLO to RDY high Delay	VCC1 Rising from 0V to 5V		15	25	us
t <sub>VCC2+_RDY</sub>	VCC2 UVLO to RDY high Delay	VCC2 Rising from 0V to 15V		40	60	us
t <sub>VCC2-_RDY</sub>	VCC2 UVLO to RDY low Delay	VCC2 Falling from 15V to 0V		220		ns
t <sub>GF</sub>	IN+, IN- signal glitch filter		20	30	40	ns
t <sub>DESAT(90%)</sub>	DESAT to 90% V <sub>OUT</sub> Delay	C <sub>LOAD</sub> =10nF		0.35	0.6	us
t <sub>DESAT(10%)</sub>	DESAT to 10% V <sub>OUT</sub> Delay	C <sub>LOAD</sub> =10nF		1.2	2.1	us
t <sub>DESAT(MUTE)</sub>	DESAT Fault Mute Time			26	35	us
t <sub>DESAT(GF)</sub>	DESAT glitch filter delay			0.15	0.25	us
t <sub>DESAT(FLT)</sub>	DESAT Fault to $\overline{\text{FLT}}$ Low Delay			0.45	0.7	us
t <sub>DESAT(RDY)</sub>	DESAT Fault to RDY Low Delay			0.45	0.7	us
t <sub>DESAT(LEB)</sub>	DESAT leading edge blanking time			0.25	0.45	us
t <sub>GFRST</sub>	Glitch filter on $\overline{\text{RST}}$ for resetting $\overline{\text{FLT}}$			0.2	0.3	us
CMT <sub>IH</sub>	Output High Level Common Mode Transient Immunity	V <sub>CM</sub> =1500V, V <sub>CC2</sub> =15V, T <sub>A</sub> =25°C	150			kV/us
CMT <sub>IL</sub>	Output Low Level Common Mode Transient Immunity	V <sub>CM</sub> =1500V, V <sub>CC2</sub> =15V, T <sub>A</sub> =25°C	150			kV/us

TYPICAL PERFORMANCE CHARACTERISTICS

T<sub>A</sub>=25°C, VCC1-GND1 = 5V, VCC2-GND2 = 15V, VEE2=GND2, C<sub>LOAD</sub>=1nF, unless otherwise specified

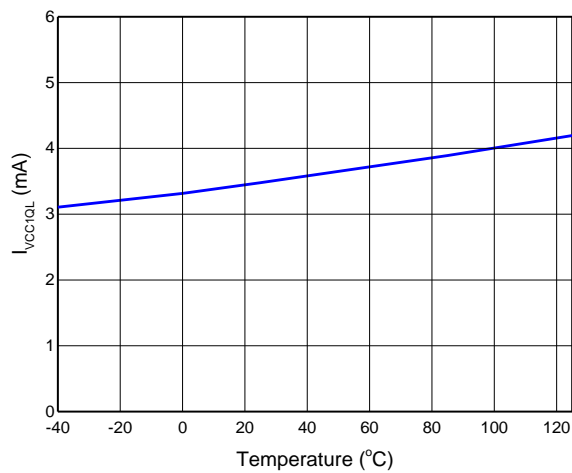


Figure 5. I<sub>VCC1QL</sub> vs Temperature

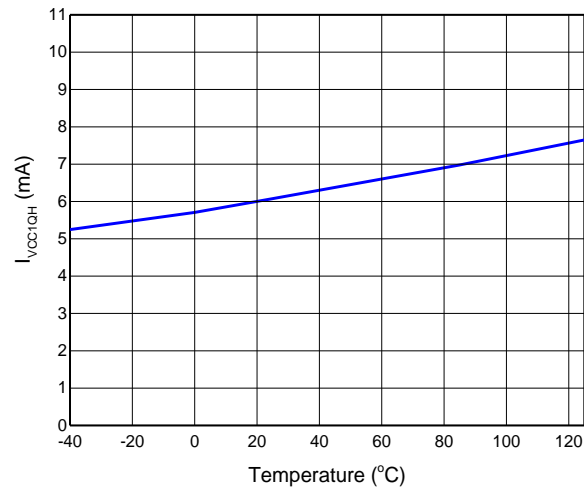


Figure 6. I<sub>VCC1QH</sub> vs Temperature

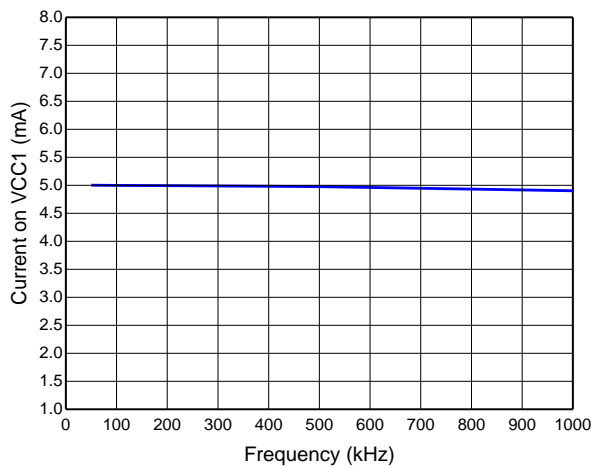


Figure 7. I<sub>VCC1</sub> vs Frequency

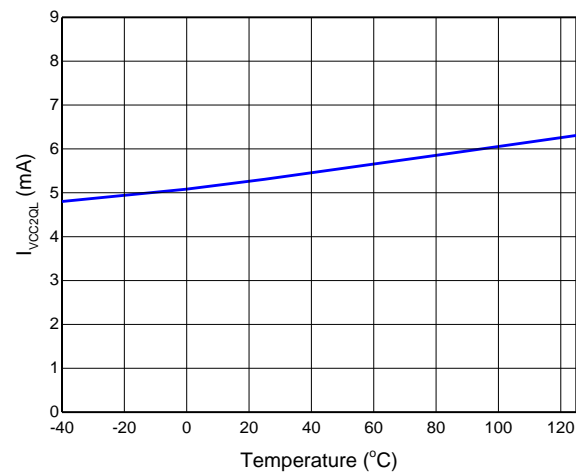


Figure 8. I<sub>VCC2QL</sub> vs Temperature

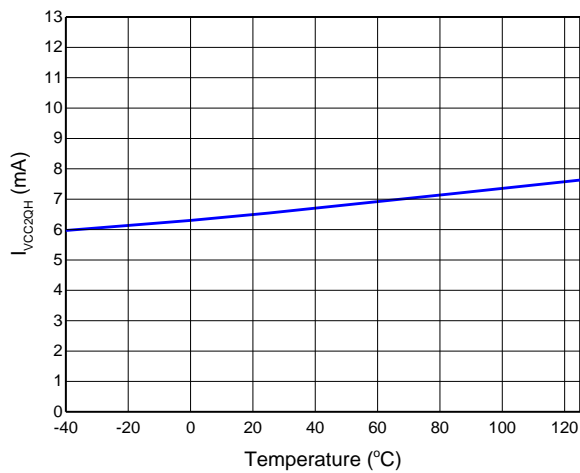


Figure 9. I<sub>VCC2QH</sub> vs Temperature

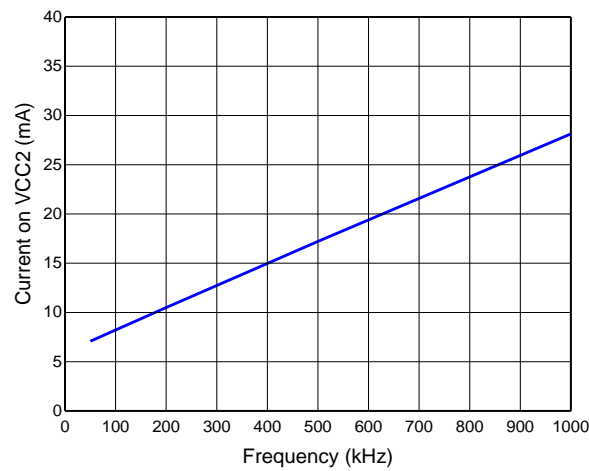


Figure 10. I<sub>VCC2</sub> vs Frequency

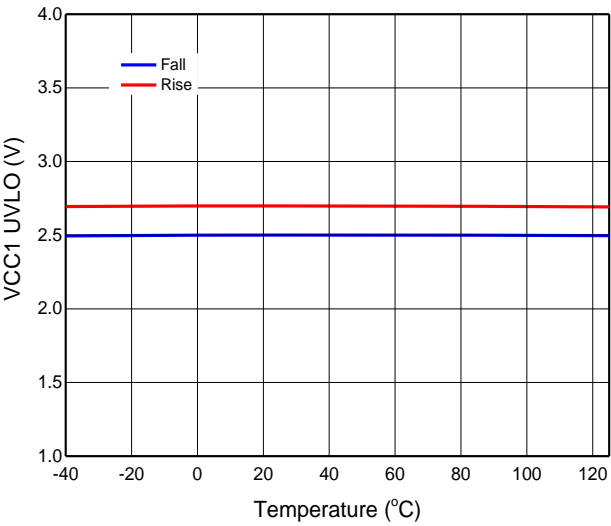


Figure 11. VCC1 UVLO vs Temperature

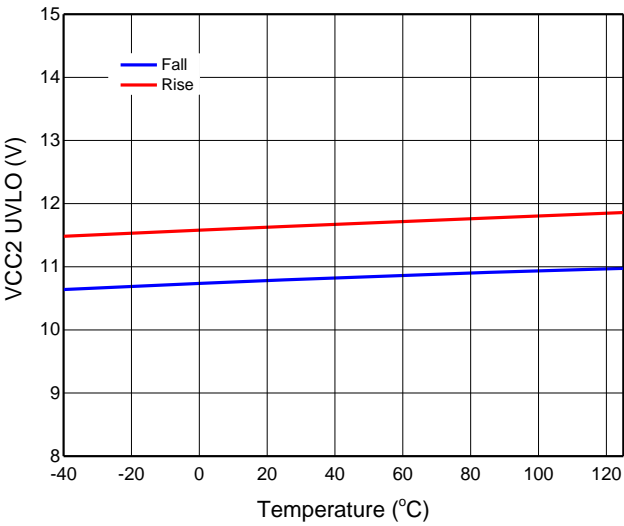


Figure 12. VCC2 UVLO vs Temperature

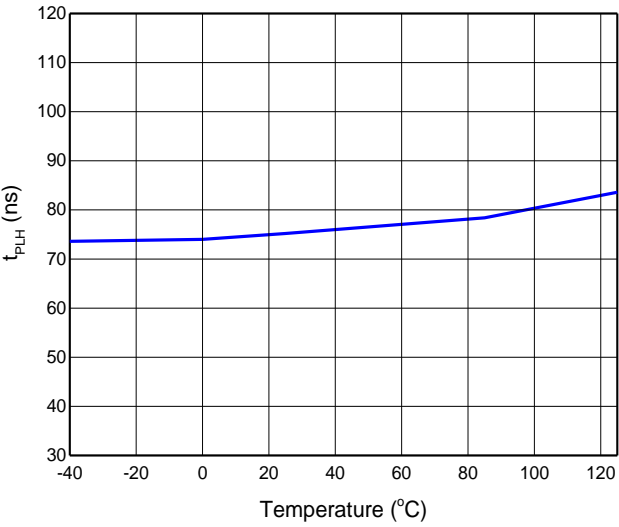


Figure 13. Propagation delay t<sub>PLH</sub> vs Temperature

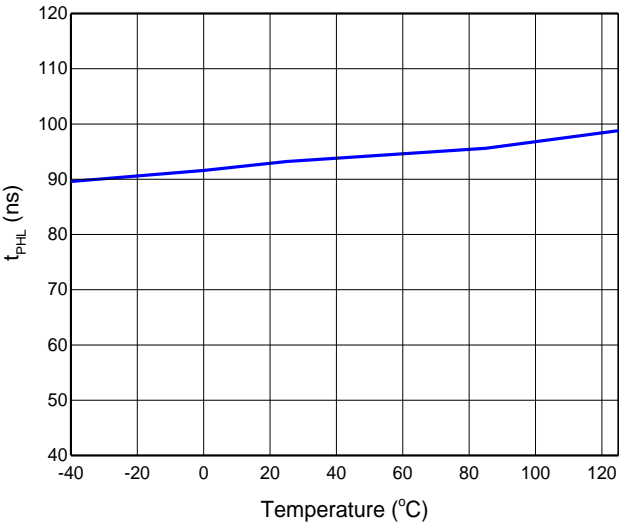


Figure 14. Propagation delay t<sub>PHL</sub> vs Temperature

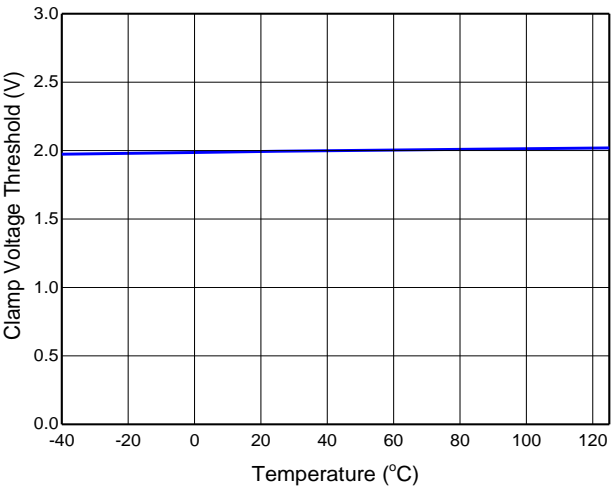


Figure 15. Clamp threshold voltage vs Temperature

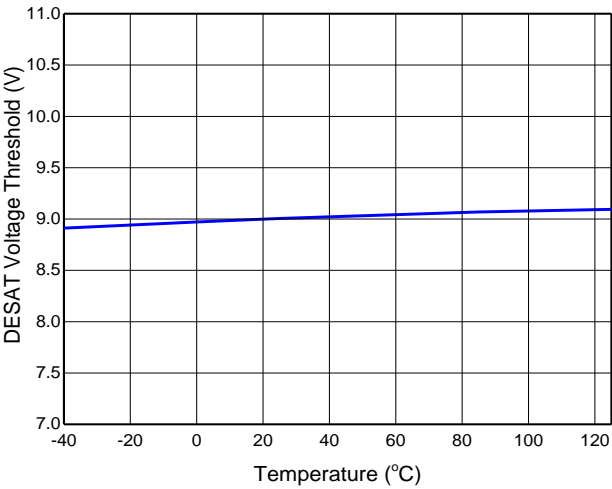


Figure 16. Desat threshold voltage vs Temperature

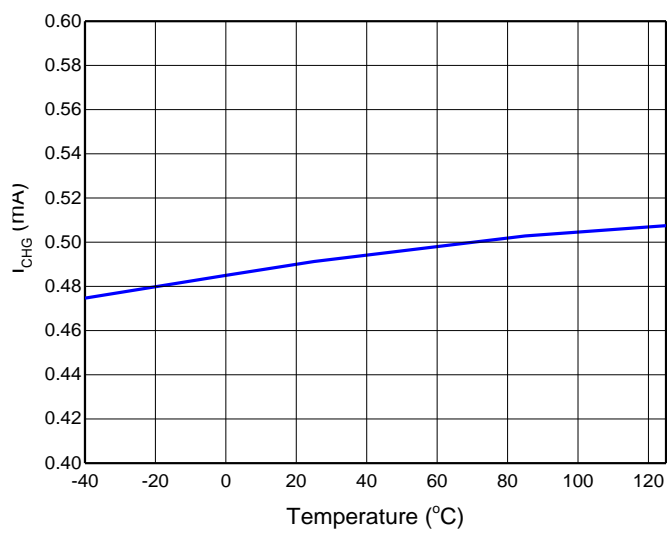


Figure 17.  $I_{CHG}$  vs Temperature

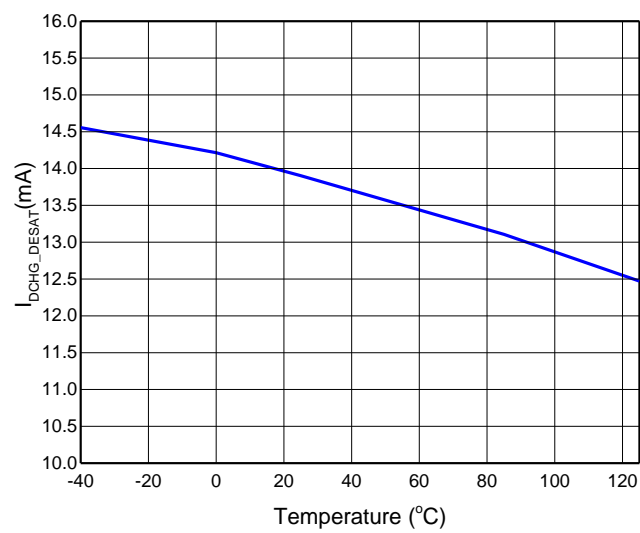


Figure 18.  $I_{DCHG\_DESAT}$  vs Temperature

## PARAMETER MEASUREMENT INFORMATION

### Propagation Delay, Rise Time and Fall Time

Figure 19 and Figure 20 shows the circuit used to measure the rise ( $t_r$ ) and fall ( $t_f$ ) times, and the propagation delays  $t_{PDLH}$  and  $t_{PDHL}$ .

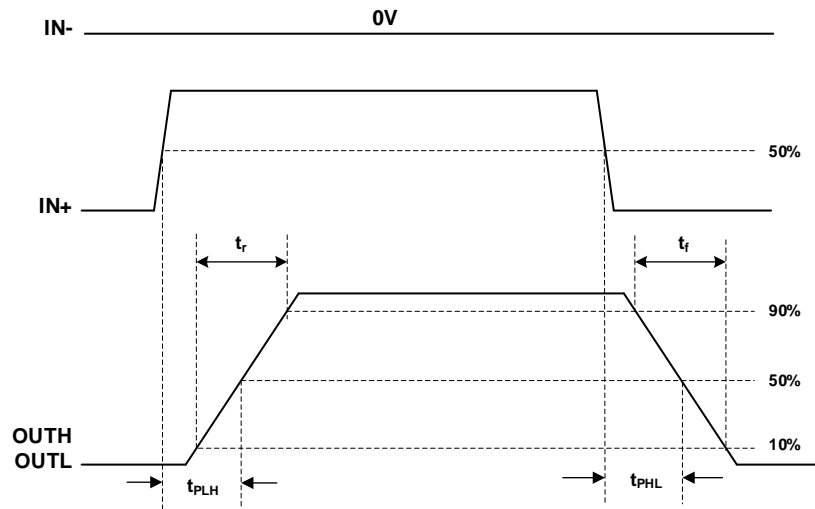


Figure 19. Propagation Delay, Rise Time and Fall Time in Noninverting Configuration

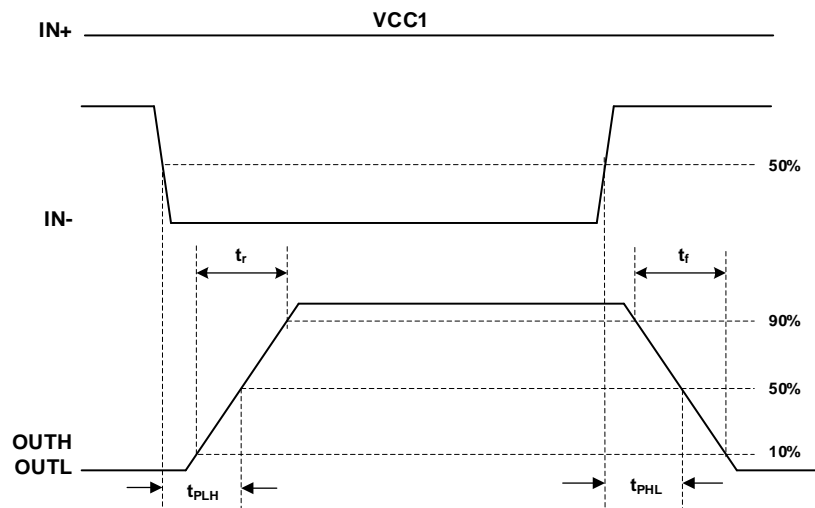


Figure 20. Propagation Delay, Rise Time and Fall Time in Inverting Configuration

### CMTI Testing

Figure 21 to Figure 24 show the simplified diagram of the CMTI testing configuration.

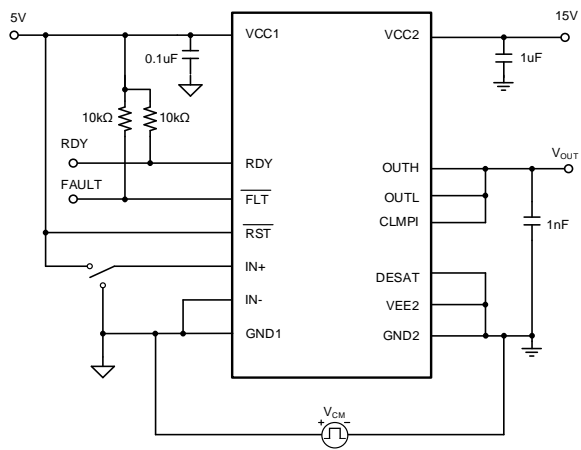


Figure 21. CMTI Test for Output

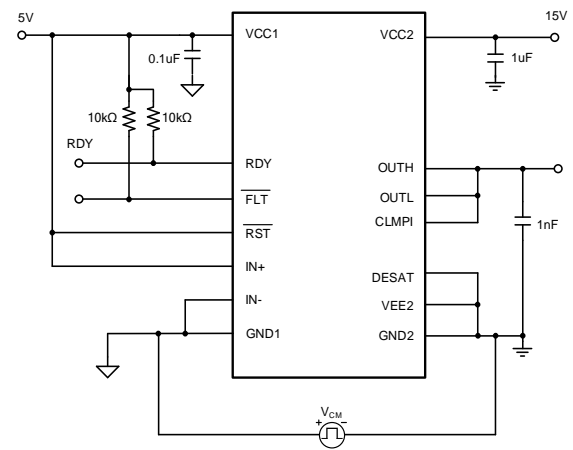


Figure 22. CMTI Test for RDY

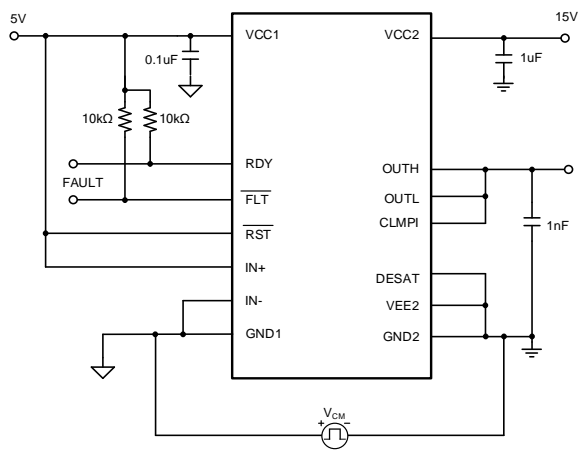


Figure 23. CMTI Test for Fault High

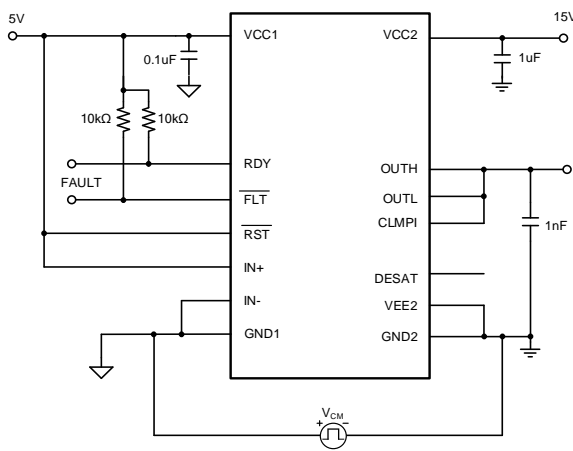


Figure 24. CMTI Test for Fault Low

Input Glitch Filter Testing

Figure 25 and Figure 26 show the IN+ pin pulse deglitch filter timing and Figure 27 and Figure 28 show the IN- pin pulse deglitch filter timing.

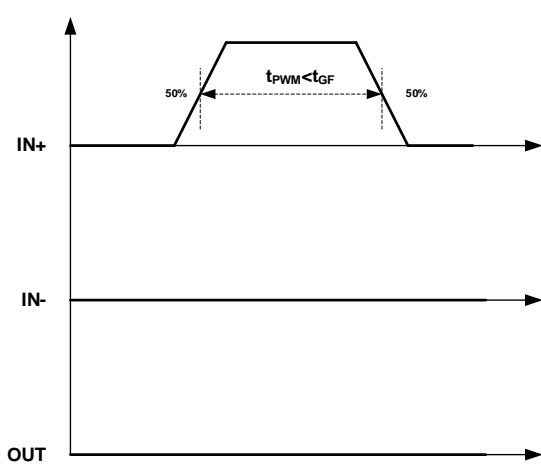


Figure 25. IN+ On Deglitch Filter

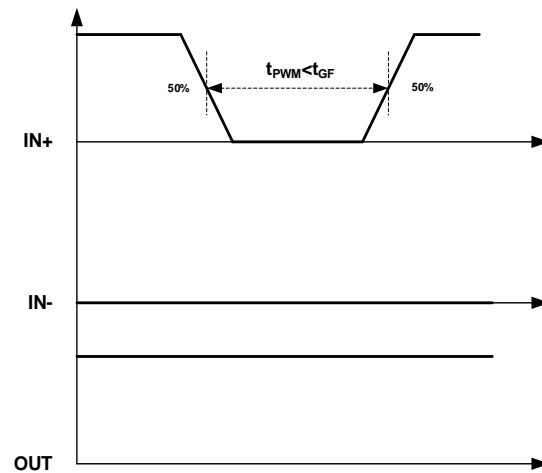


Figure 26. IN+ Off Deglitch Filter



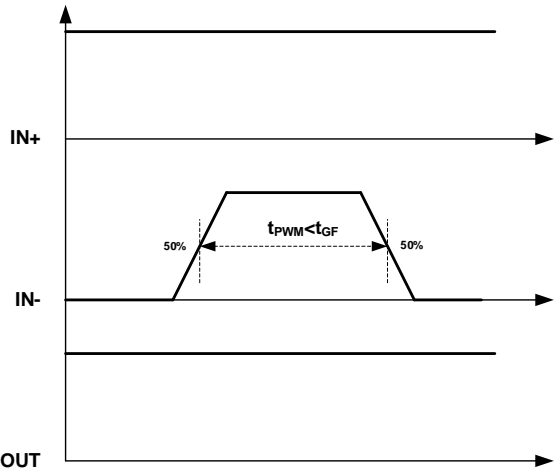


Figure 27. IN- On Deglitch Filter

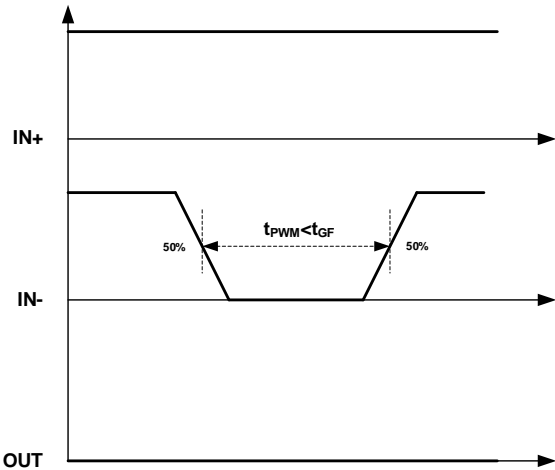


Figure 28. IN- Off Deglitch Filter

## FEATURE DESCRIPTION

The SiLM5852SH-AQ is an advanced input CMOS logic single channel isolated gate driver with rich protection features, such as desaturation detection, miller clamp, isolated fault sensing and under voltage lockout.

### UVLO with RDY Pin Indication

The IGBT is turned off if either supply VCC1 or VCC2 drops below UVLO threshold irrespective to other logic control signals. RDY pin indicates status of input and output side UVLO internal protection feature. If either side of device have insufficient supply (VCC1 or VCC2), the RDY pin output goes low; otherwise, RDY pin output is high. RDY pin also serves as an indication to the micro-controller that the device is ready for operation.

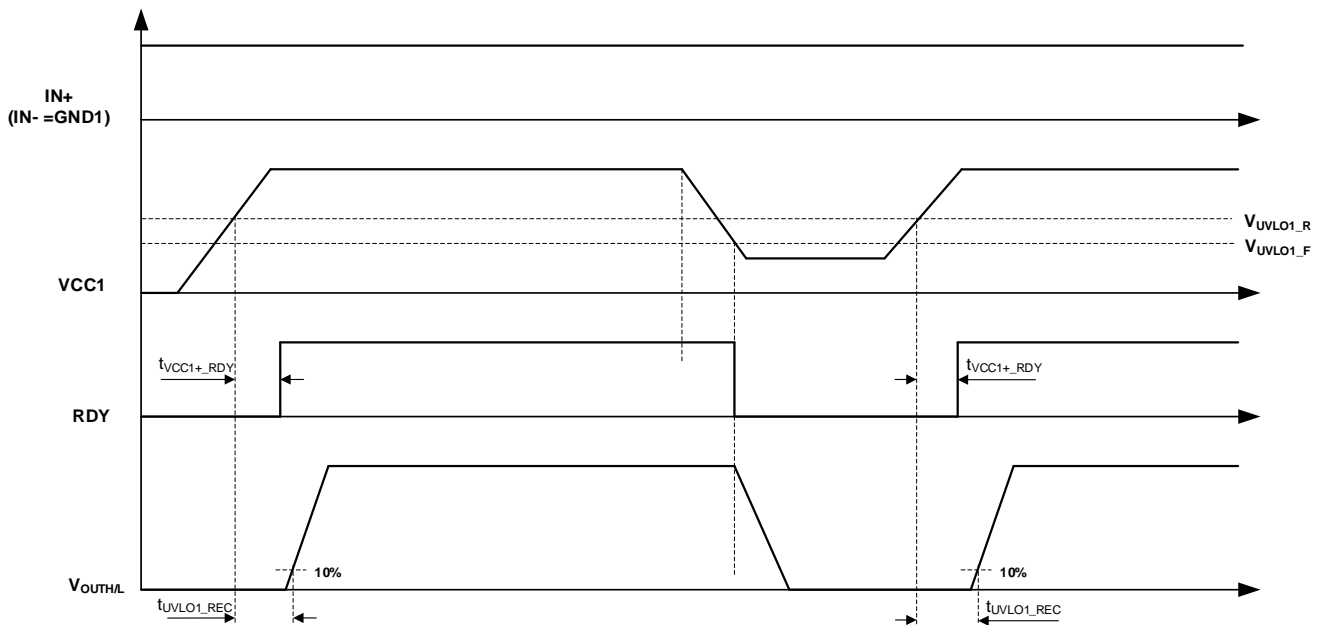


Figure 29.VCC1 UVLO Protection Timing

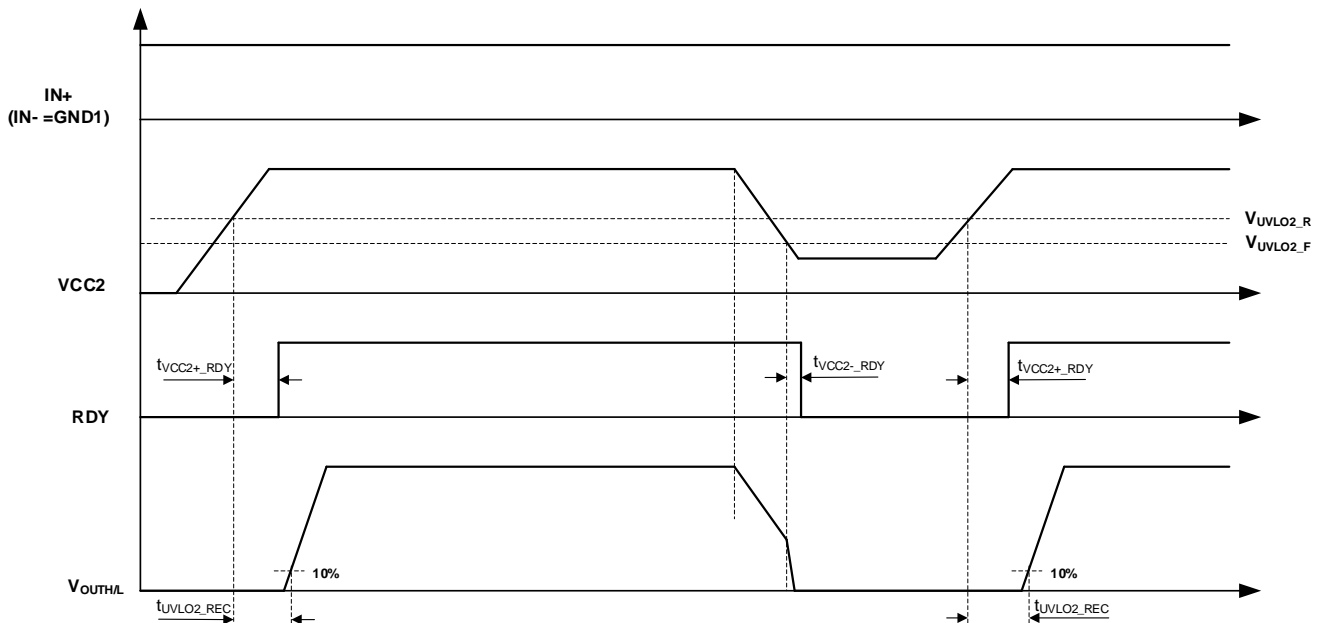


Figure 30.VCC2 UVLO Protection Timing

## Fault Sensing and Reset

The SiLM5852SH-AQ integrates isolated fault indication. When the DESAT has monitored a fault on the IGBT, it also activates an internal feedback channel which pull low the  $\overline{\text{FLT}}$  and RDY pin in the input side to inform the fault condition to a micro-controller. In the meanwhile, all input control signals will be ignored during the fault period to allow the driver to completely shutdown the IGBT. The driver will automatically reset the RDY pin after a fixed mute time,  $t_{\text{DESAT(MUTE)}}$ . The  $\overline{\text{FLT}}$  output condition is latched and can only be reset after RDY goes high, through an active-low pulse at the  $\overline{\text{RST}}$  input.  $\overline{\text{RST}}$  has an internal filter to reject noise and glitches. By asserting  $\overline{\text{RST}}$  for at least the specified minimum duration,  $t_{\text{GFRST}}$ , device input logic can be enabled or disabled.

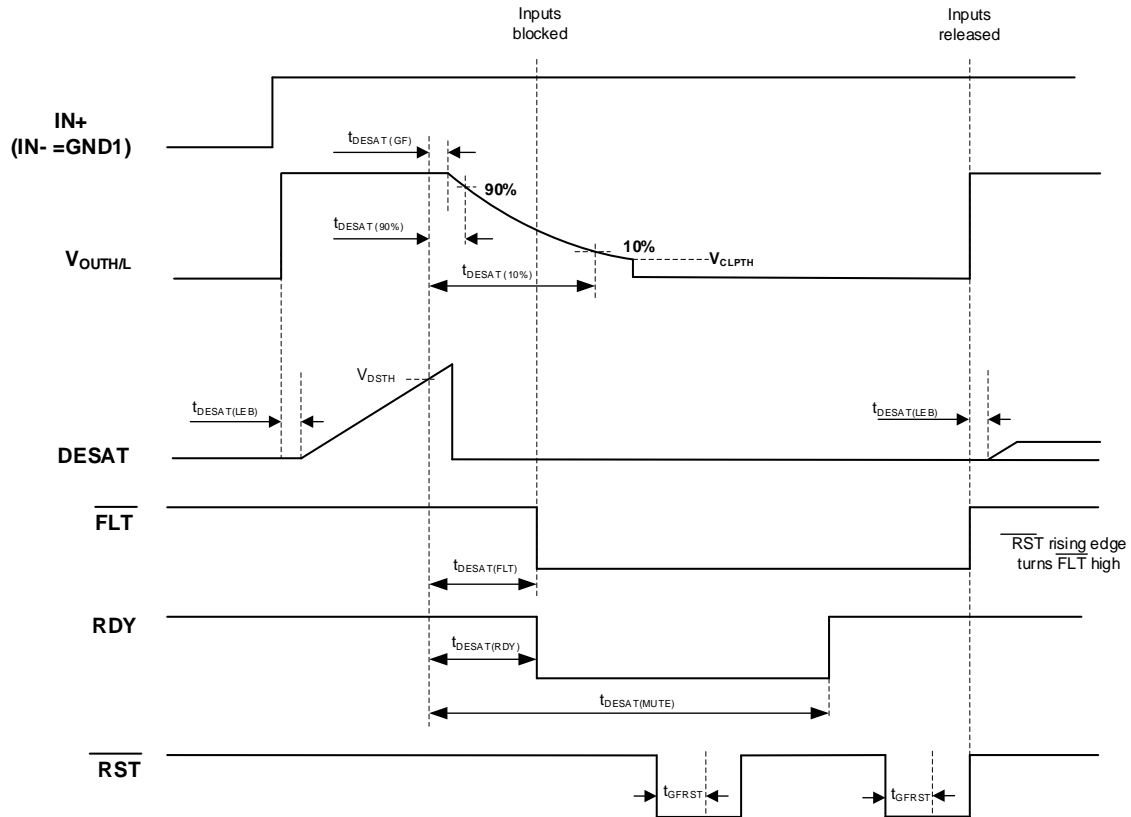


Figure 31.  $\overline{\text{FLT}}$ , RDY and  $\overline{\text{RST}}$  Timing Diagram

## Desaturation Detection

The DESAT pin monitors the IGBT  $V_{\text{CE}}$  voltage. When the voltage on the DESAT pin exceeds DESAT threshold 9V while the IGBT is on, the output will be pulled down.

A blank time is needed in the DESAT detection circuit following the turn on of the IGBT to allow the collector voltage to fall below the DESAT threshold. The blank time is controlled by the internal DESAT blank charge current, the DESAT voltage threshold, and the external DESAT capacitor. Using the following equation to calculate the blank time.

$$t_{\text{BLANK}} = \frac{C_{\text{BLANK}} \times V_{\text{DSTH}}}{I_{\text{CHG}}}$$

Here:

$t_{\text{BLANK}}$ : Blank time

$C_{\text{BLANK}}$ : External DESAT capacitor

$V_{\text{DSTH}}$ : DESAT threshold voltage

$I_{\text{CHG}}$ : Blank capacitor charging current

During the IGBT turn on, high negative spike voltage occurs on the collection of the IGBT due to parasitic parameters and this negative spike may damage the DESAT pin. In order to protect the DESAT pin in such case, a resistor,  $R_{DST}$ , is needed to be in series with the DESAT diode. The value of the  $R_{DST}$  depends on the different application, but generally a  $100\Omega$  resistor is recommended. Further protection is possible through an optional Schottky diode to clamp the DESAT input to GND2 at low voltage levels with its low forward voltage.

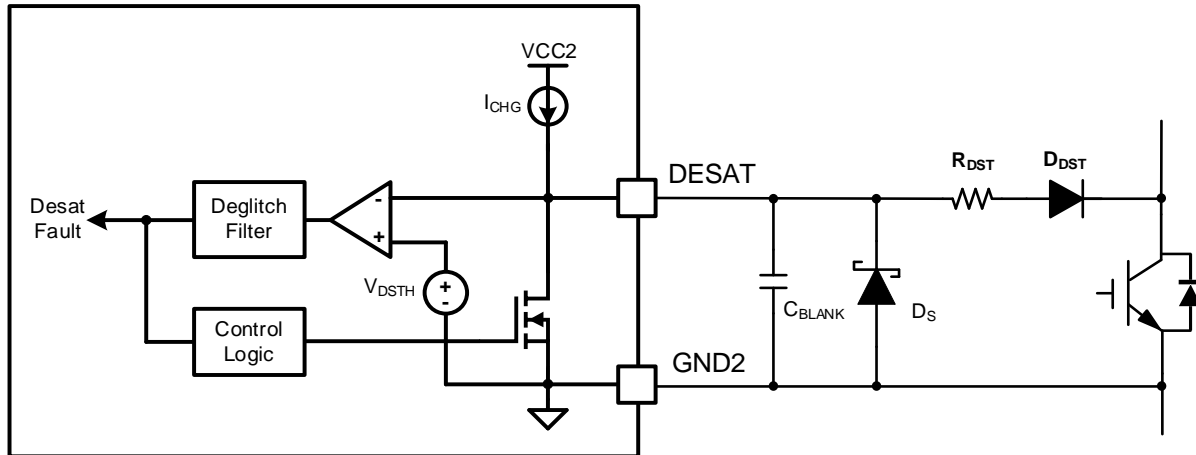


Figure 32. DESAT Protection

## Soft Turn Off

SiLM5852SH-AQ initiates a soft turn-off when the short circuit protection is triggered. When the short circuit fault happens, the IGBT transits from the active region to the desaturation region very fast. The channel current is controlled by the gate voltage and decreasing in a soft manner, thus the overshoot of the IGBT is limited and prevents the overvoltage breakdown. The turn off speed needs to be slow to limit the overshoot voltage, but the shutdown time should not be too long that the large energy dissipation can breakdown the device. The soft turn off current ( $I_{OLF}$ ) of SiLM5852SH-AQ makes sure the power switches are safely turned off during short circuit events.

## Internal Active Miller Clamp

A Miller clamp circuit integrates in the SiLM5932SH which allows the control of the Miller current during a high  $dV/dt$  situation and can eliminate the use of a negative supply voltage in most of the applications. During turn off, the gate voltage is monitored through the OUTH pin and the clamp circuit is activated when the voltage on the OUTH pin goes below the clamp voltage threshold,  $V_{CLMTH}$ , (2V typical, relative to VEE2). A clamp low sink current is generated when the clamp circuit is activated. The clamp circuit is disabled when the input on signal is triggered again. In order to achieve good clamping results, the CLMPI shall connect to the gate of the power device, close to the power device on the PCB layout.

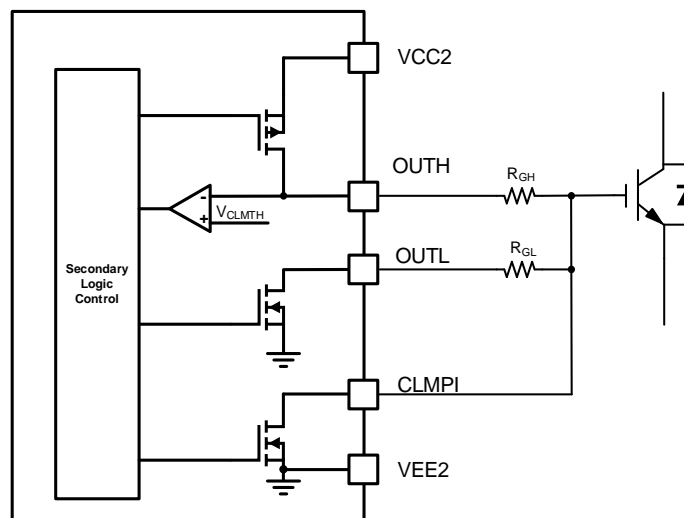
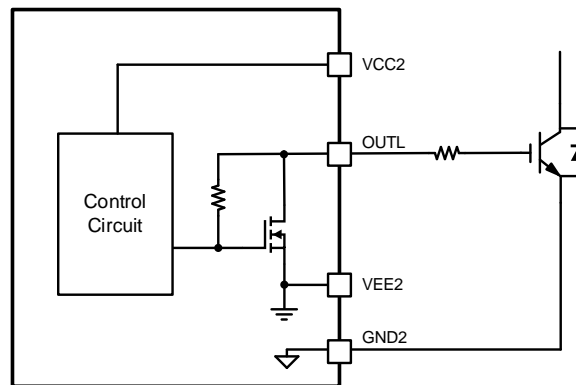


Figure 33. Active Miller Clamp

## Active Output Pulldown

The Active output pulldown feature ensures that the IGBT gate OUTH/L is clamped to VEE2 to ensure safe IGBT off-state, when VCC2 is open.



### Figure 34. Active Output Pulldown

## Short Circuit Clamping

Under short circuit events it is possible that currents are induced back into the gate-driver OUTH/L and CLMPI pins due to parasitic Miller capacitance between the IGBT collector and gate terminals. Internal protection diodes on OUTH/L and CLMPI help to sink these currents while clamping the voltages on these pins to values slightly higher than the output side supply.

## Input Deglitch Filter

In order to increase the robustness of gate driver over noise transient and accidental small pulses on the input pins, such as, a  $t_{GF}$  deglitch filter on IN+, IN– and, a  $t_{GFRST}$  deglitch filter on  $\overline{RST}$  is designed to filter out the transients and make sure there is no faulty output responses or accidental driver malfunctions. When the IN+ or IN– PWM pulse is smaller than the input deglitch filter width, there will be no responses on drive signal.

## Device Functional Modes

Table 1. SiLM5852SH-AQ function table

VCC1	VCC2	VEE	IN+	IN-	$\overline{\text{RST}}$	RDY	$\overline{\text{FLT}}$	OUTH/OUTL	CLMPI
PU	PD	PU	X	X	X	Low	HiZ	Low	Low
PD	PU	PU	X	X	X	Low	HiZ	Low	Low
PU	PU	PU	X	X	Low	HiZ	HiZ	Low	Low
PU	PU	PU	Low	X	High	HiZ	HiZ	Low	Low
PU	PU	PU	X	High	High	HiZ	HiZ	Low	Low
PU	PU	PU	High	Low	High	HiZ	HiZ	High	HiZ

PU: Power up, voltage higher than UVLO, PD: Power down, voltage lower than UVLO, HiZ, High impedance

## LAYOUT

In order to achieve optimum performance for the SiLM5852SH-AQ, some suggestions on the PCB layout.

Component placement:

- Low-ESR capacitors must be connected close to the device between the  $V_{CC2}$  and  $V_{EE}$  pins to bypass noise and to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the  $V_{EE}$  pins connected to the switch node, the parasitic inductances between the source of the top transistor and the drain of the bottom transistor must be minimized.

Grounding considerations:

- Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. Small trace loop decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.

High-voltage considerations:

- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.

PACKAGE CASE OUTLINES

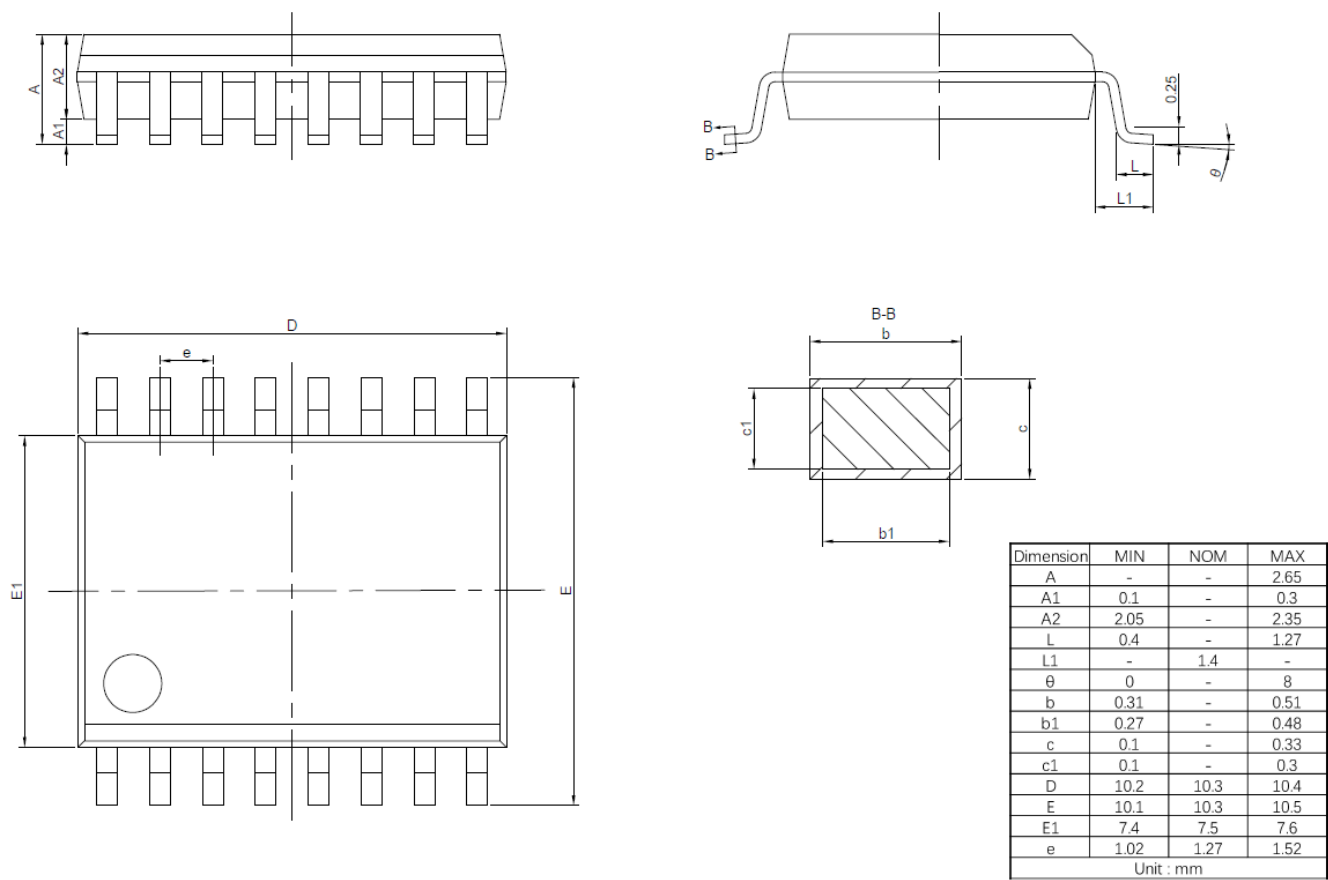


Figure 35. SOP16W Package Outline Dimensions